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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,927	03/16/2004	Akiyoshi Aoyagi	9319S-000669	2334

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,927	AOYAGI, AKIYOSHI	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3,6,7/04,3,4,5/05.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the filing of the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 discloses an elastic modulus of the first carrier and chip different from the elastic modulus of the second carrier and chip, it is unclear how this is attained and how temperature is related to the elasticity. The specification does not disclose this limitation clearly.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 7 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoyagi (U.S. Publication 2004/0135243).

Aoyagi discloses a semiconductor device (Fig. 3) that contains a first carrier substrate (10), a first semiconductor chip (11) mounted face down on the first carrier substrate, a second carrier substrate (30), a second semiconductor chip (31) mounted on the second carrier substrate, protruding electrodes (32) for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first semiconductor chip; a sealant comprising mold resin sealing the second semiconductor chip, the second carrier substrate is fixed to the first carrier substrate so as to be mounted on the first semiconductor chip, a resin (18) provided between the first carrier and second carrier so the reverse face of the first semiconductor is exposed, the position of a sidewall of the sealant coincides with a sidewall of the second carrier substrate, the first carrier substrate comprises a flip-chip mounted ball grid array and the second carrier substrate comprises a mold-sealed ball grip array and chip size package, the first semiconductor chip comprises a plurality of chips mounted in parallel on the first carrier substrate (15b/15c), the second semiconductor chip comprise a plurality of stacked semiconductor chips (14b/14c) and in parallel with second carrier substrate.

Claim 11 is rejected under 35 U.S.C. 102(e) as being anticipated by Nishimura.

Nishimura discloses a semiconductor device (Fig. 16) that contains a first carrier substrate (1b), a first semiconductor chip (3b) mounted face down on the first carrier substrate, a second carrier substrate (1a), a second semiconductor chip (3c) mounted on the second carrier substrate with re-arrangement wiring lines (area where wires are bonded to second carrier substrate) are formed on surfaces where electrode pads (electrodes between wire bond areas), protruding electrodes (7) for connecting the second semiconductor chip to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first semiconductor chip.

Claims 12 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoyagi (U.S. Publication 2004/0135243).

Aoyagi discloses a semiconductor device (Fig. 3) that contains a first carrier substrate (10), a first electronic part (11) mounted face down on the first carrier substrate, a second carrier substrate (30), a second electronic part (31) mounted on the second carrier substrate, protruding electrodes (32) for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first electronic part; a sealant comprising mold resin sealing the second electronic part, the second carrier substrate is fixed to the first carrier substrate so as to be mounted on the first electronic part, a resin (18) provided between the first carrier and second carrier so the reverse face of the first electronic part is exposed.

Claim 13 is rejected under 35 U.S.C. 102(e) as being anticipated by Aoyagi (U.S. Publication 2004/0135243).

Aoyagi discloses a semiconductor device (Fig. 3) that contains a first carrier substrate (10), a first semiconductor chip (11) mounted face down on the first carrier substrate, a second carrier substrate (30), a second semiconductor chip (31) mounted on the second carrier substrate, protruding electrodes (32) for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first semiconductor chip; a sealant comprising mold resin sealing the second semiconductor chip, the second carrier substrate is fixed to the first carrier substrate so as to be mounted on the first semiconductor chip, a resin (18) provided between the first carrier and second carrier so the reverse face of the first semiconductor chip is exposed and a mother substrate on which the first carrier substrate is mounted (dash lines in fig. 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (U.S. Patent 6,781,241) in view of Aoyagi.

Nishimura discloses a semiconductor device (Figs. 8 and 16) that contains a first carrier substrate (1b), a first semiconductor chip (3b) mounted face down on the first carrier substrate, a second carrier substrate (1a), a second semiconductor chip (3c)

mounted on the second carrier substrate, protruding electrodes (7) for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first semiconductor chip; a sealant (2) comprising mold resin sealing the second semiconductor chip, the second carrier substrate is fixed to the first carrier substrate so as to be mounted on the first semiconductor chip, the position of a sidewall of the sealant coincides with a sidewall of the second carrier substrate, the first carrier substrate comprises a flip-chip mounted ball grid array and the second carrier substrate comprises a mold-sealed ball grip array and chip size package, the first semiconductor chip comprises a plurality of chips mounted in parallel on the first carrier substrate (Fig. 8), the second semiconductor chip comprise a plurality of stacked semiconductor chips and in parallel with second carrier substrate. In regards to the first semiconductor chip connected to the first carrier substrate by pressure welding, a *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear. Even though product –by [-] process claims are limited by and defined by the process, determination of patentability is based upon

the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted)." Nishimura discloses all the limitations except for a resin provided between the first carrier and second carrier so the reverse face of the first semiconductor is exposed. Whereas Aoyagi discloses a semiconductor device (Fig. 3) that contains a first carrier substrate (10) and second carrier (30) with a first semiconductor chip (11) mounted on first carrier substrate with a resin (18) provided between the first and second carrier substrate so the reverse face of the first semiconductor chip is exposed. The resin is formed on the first semiconductor chip to seal and encapsulate the first semiconductor chip. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Nishimura by incorporating a resin between the first and second carrier substrate to encapsulate and seal the first semiconductor chip as taught by Aoyagi.

Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (U.S. Patent 6,781,241) in view of Aoyagi.

Nishimura discloses a semiconductor device (Figs. 8 and 16) that contains a first carrier substrate (1b), a first electronic part (3b) mounted face down on the first carrier substrate, a second carrier substrate (1a), a second electronic part (3c) mounted on the second carrier substrate, protruding electrodes (7) for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above

and spaced apart from the first electronic part; a sealant (2) comprising mold resin sealing the second electronic part. Nishimura discloses all the limitations except for a resin provided between the first carrier and second carrier so the reverse face of the first electronic part is exposed. Whereas Aoyagi discloses a semiconductor device (Fig. 3) that contains a first carrier substrate (10) and second carrier (30) with a first electronic part (11) mounted on first carrier substrate with a resin (18) provided between the first and second carrier substrate so the reverse face of the first electronic part is exposed. The resin is formed on the first electronic part to seal and encapsulate the first electronic part. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Nishimura by incorporating a resin between the first and second carrier substrate to encapsulate and seal the first electronic part as taught by Aoyagi.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (U.S. Patent 6,781,241) in view of Aoyagi.

Nishimura discloses a semiconductor device (Figs. 8 and 16) that contains a first carrier substrate (1b), a first semiconductor chip (3b) mounted face down on the first carrier substrate, a second carrier substrate (1a), a second semiconductor chip (3c) mounted on the second carrier substrate, protruding electrodes (7) for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first semiconductor chip; a sealant (2) comprising mold resin sealing the second semiconductor chip and a mother substrate on which the first carrier substrate is mounted (Column 5, lines 58-61) . Nishimura

discloses all the limitations except for a resin provided between the first carrier and second carrier so the reverse face of the first semiconductor chip is exposed. Whereas Aoyagi discloses a semiconductor device (Fig. 3) that contains a first carrier substrate (10) and second carrier (30) with a first semiconductor chip (11) mounted on first carrier substrate with a resin (18) provided between the first and second carrier substrate so the reverse face of the first semiconductor chip is exposed. The resin is formed on the first electronic part to seal and encapsulate the first semiconductor chip. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Nishimura by incorporating a resin between the first and second carrier substrate to encapsulate and seal the first semiconductor chip as taught by Aoyagi.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura, Aoyagi and Wachtler (U.S. Publication 20030022465).

Nishimura and Aoyagi disclose all the limitations except for the second chips molded and cut. Whereas Wachtler discloses wafer package (Figs. 16 and 17) that contains semiconductor chips (204) integrally molded on a carrier substrate (134) with a sealing resin where the carrier substrate is cut with the sealing resin so each piece includes one semiconductor chip. The carrier substrate is cut so as to produce individual molded chip for integrated circuit packages. (Page 6, Paragraph 62) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Nishimura and Aoyagi by incorporating

cutting the carrier with the molded semiconductor chip to produce individual molded chip for integrated circuit packages as taught by Wachtler.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyagi in view of Wachtler (U.S. Publication 20030022465).

Aoyagi discloses all the limitations except for the second chips molded and cut. Whereas Wachtler discloses wafer package (Figs. 16 and 17) that contains semiconductor chips (204) integrally molded on a carrier substrate (134) with a sealing resin where the carrier substrate is cut with the sealing resin so each piece includes one semiconductor chip. The carrier substrate is cut so as to produce individual molded chip for integrated circuit packages. (Page 6, Paragraph 62) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Aoyagi by incorporating cutting the carrier with the molded semiconductor chip to produce individual molded chip for integrated circuit packages as taught by Wachtler.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

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